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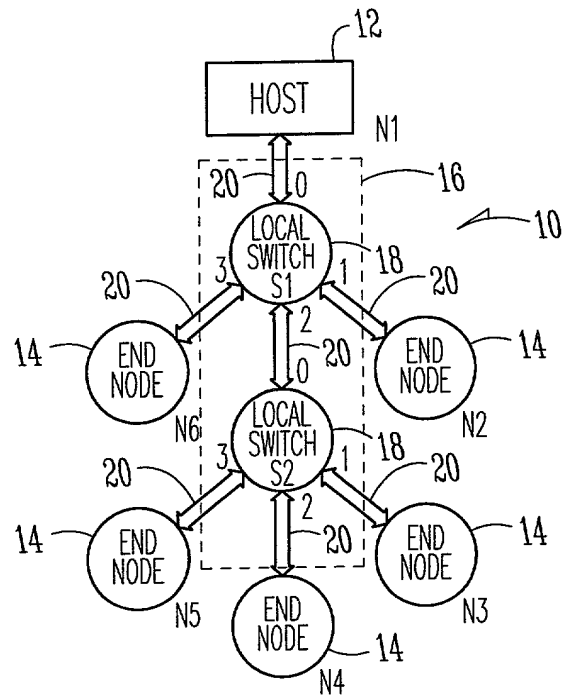


Fig. 1

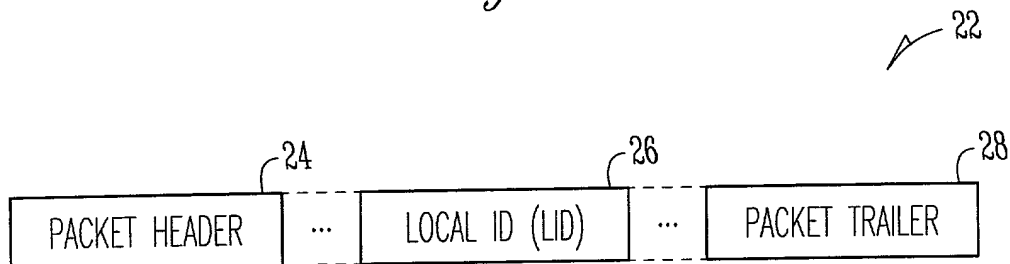


Fig. 2

S1 LOCAL		S2 LOCAL	
NODE	PORT	NODE	PORT
N1	0	N1	0
N2	1	N2	0
N3	2	N3	1
N4	2	N4	2
N5	2	N5	3
N6	3	N6	0

Fig. 3

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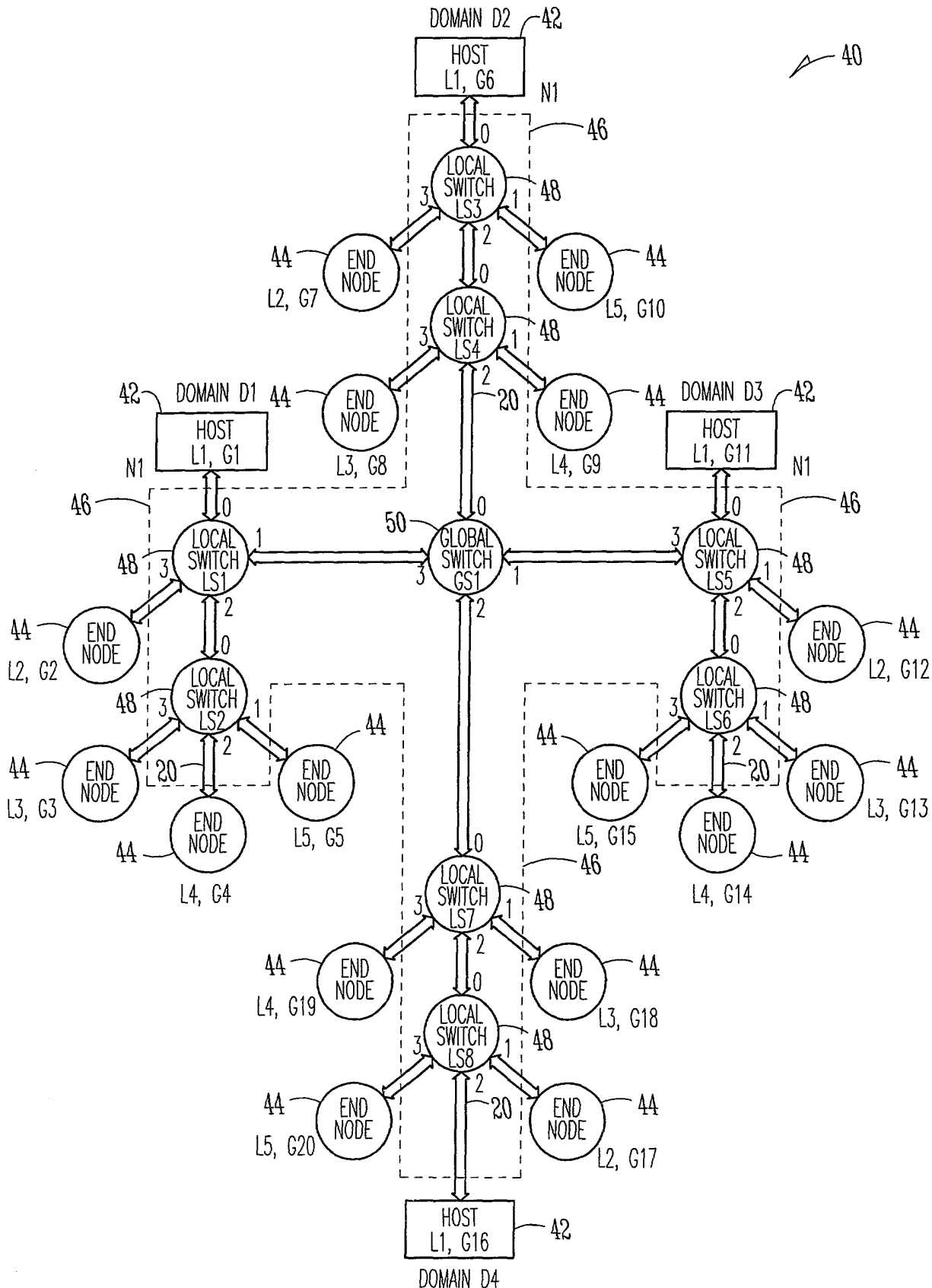


Fig. 4

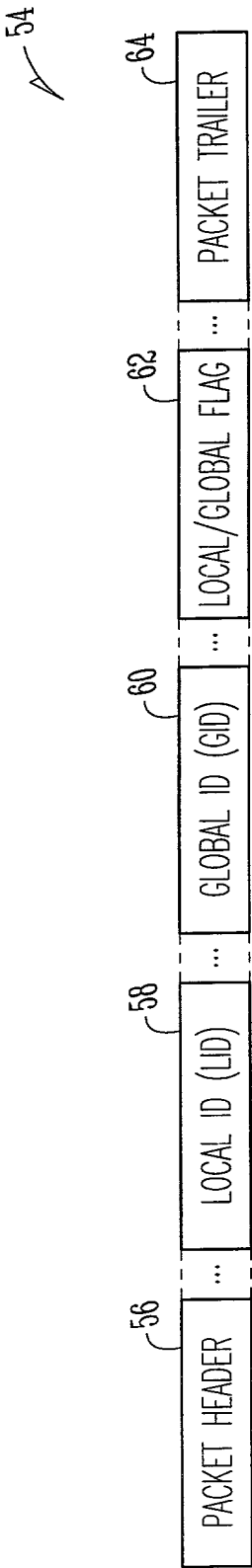


Fig. 5

TITLE: MULTIPLE-DOMAIN PROCESSING SYSTEM USING HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

INVENTORS NAME: Oleg Awsienko et al.
SERIAL NO.: 10/005,895

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LS3 LOCAL		LS3 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D1	2
L2	3	D3	2
L3	2	D4	2
L4	2		
L5	1		

LS4 LOCAL		LS4 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D1	2
L2	0	D3	2
L3	3	D4	2
L4	2		
L5	0		

LS1 LOCAL		LS1 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D2	1
L2	3	D3	1
L3	2	D4	1
L4	2		
L5	2		

LS2 LOCAL		LS2 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D2	0
L2	0	D3	0
L3	3	D4	0
L4	2		
L5	5		

LS5 LOCAL		LS5 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D1	3
L2	1	D2	3
L3	2	D4	3
L4	2		
L5	2		

LS6 LOCAL		LS6 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	0	D1	0
L2	0	D2	0
L3	1	D4	0
L4	2		
L5	3		

CS1 GLOBAL	
DOMAIN	PORT
D1	3
D2	0
D3	1
D4	2

LS7 LOCAL		LS7 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	2	D1	0
L2	2	D2	0
L3	1	D3	0
L4	3		
L5	2		

LS8 LOCAL		LS8 GLOBAL	
NODE	PORT	DOMAIN	PORT
L1	2	D1	0
L2	1	D2	0
L3	0	D3	0
L4	0		

Fig. 6

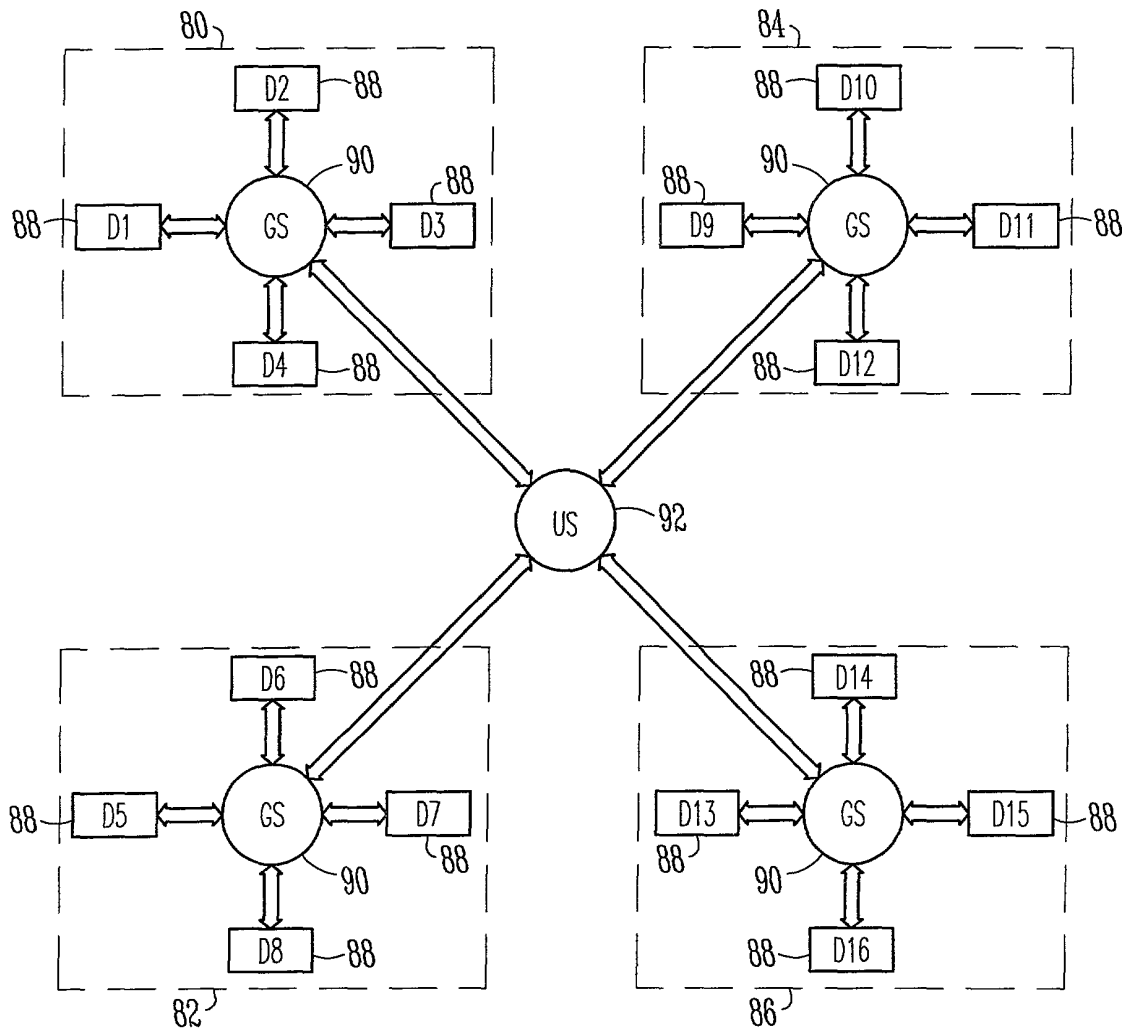


Fig. 7